RADCOM TECHNICAL FEATURE

A Practical Synthesizer

for ex-PMR VHF Transceivers

The first of a two part article by Bernie Pallett, G3VML

FOR THE NEWLY LICENSED amateur, or especially those of limited financial means, a major problem is often the ability to purchase new or second hand radio equipment within an affordable price range.

One source of cheap, but at the same time well constructed, VHF/UHF transceiver equipment is the surplus Private Mobile Radio (PMR) market. However the main drawbacks with this type of equipment is that the transceivers are usually limited to around three crystal controlled transmit/receive channels.

Another drawback is the cost of the crystals (about £5 each), and usually a pair of crystals are required for each channel. The cost of fitting crystals for all three channels can amount to around £30. Thus the use of ex-PMR equipment for amateur use can appear unattractive at first glance.

With these factors in mind I set out to establish whether it was possible to develop and construct an economical synthesizer circuit, that could derive the full 80 (25kHz spaced) channels of the two metre band, when used in conjunction with a surplus PMR VHF transceiver at a cost that roughly equates to the cost of six crystals. The circuit that I eventually developed, for use with a surplus Dymar type 882 high band FM transceiver, is based on the Motorola Synthesizer IC type MC145151P.

DYMAR VHF TRANSCEIVER TYPE 882

IT IS OUTSIDE THE SCOPE of this project to discuss in detail all the various makes and models of ex-PMR VHF Transceiver equipment being offered for sale on the surplus market, however many of these have a number of common features.

The Dymar high band type 882 VHF Transceiver, which was donated for this project, is fairly typical of this type of equipment, and therefore I will refer to it throughout this feature. The transceiver was designed to operate in the 146MHz to 174MHz frequency range. The receiver portion, which employs a 10.7MHz first IF stage, also has a 12.5kHz channel separation capability. The transmit master oscillator and the receiver first local oscillator are each derived from their respective crystal controlled oscillators, via x 12 (4 x 3) frequency multiplier circuits.

The formulae used to derive these crystal frequencies are:

(1) TX Crystal frequency = (Transmit frequency)/12

(2) RX Crystal frequency = (Receive frequency - IF frequency)/12

Whilst operating within the original design frequency band, the frequency tracking limits of the first local oscillator, will be 135.3MHz to 163.3MHz. The frequency limits of the amateur 2 metre band are from 144MHz to 146MHz, therefore the local oscillator frequency limits to cover this band will be 133.3MHz to 135.3MHz. If on the other hand the local oscillator were to track an IF (10.7MHz) difference above the received signal frequency, then the local oscillator would be required to track 154.7MHz to 156.7MHz. Because the higher local oscillator tracking frequencies fall well within the original frequency band of the x12 frequency multiplier circuits, this mode of oscillator tracking was chosen for the synthesizer project.

To replace crystal control by a frequency synthesizer circuit, will require the synthesizer to generate a range of frequencies around 12MHz (transmit), or 13.0583MHz (receive). An ultimate transceiver channel spacing of 12.5kHz, will equate to a step size of 12.5kHz/12 or 1041.6667Hz at the synthesizer output.

BASIC FREQUENCY SYNTHESIZER PRINCIPLES.

THE BASIC SYNTHESIZER block diagram is given in **Fig 1**, and it is possible to select a given number of 1041.6667Hz-spaced spot frequencies, within a frequency range of 12 to 13.058MHz. The resonant frequency of the Voltage Controlled Oscillator (VCO), is dependent upon an applied DC tuning voltage, derived from the phase detector. The higher resonant VCO frequencies coincide with the higher tuning voltages, whereas for the lower resonant VCO frequencies, the tuning voltage levels will be lower.

It is common practice to include a buffer amplifier between the VCO and any external circuit loads, thereby ensuring that the VCO is not pulled off frequency by possible external load changes. The phase detector has two inputs, the first is a 1041.6667Hz waveform, (the reference frequency) that is derived from a stable 8.5333MHz crystal oscillator via a divide-by-8,192 frequency divider.

The second waveform, referred to here as the variphase, is derived from the VCO via a programmable frequency divider circuit. If a frequency difference exists between the two inputs of the phase detector, a voltage ramp will be generated at the phase detector output, which in turn will cause the VCO to frequency sweep.

Because one VCO output is fed to the input of the divide-by-N frequency divider, depending upon the selected divider ratio, there will come a point where the two waveforms present at the input of the phase detector match. When a phase match of the two input waveforms has been reached, the tuning voltage at

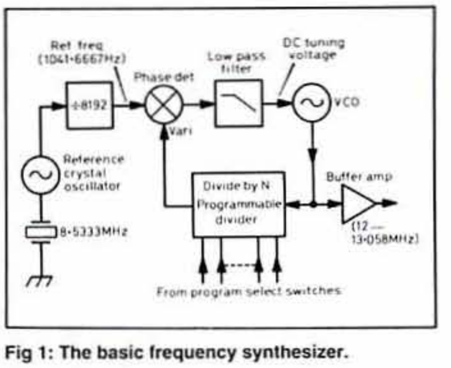


Fig 1: The basic frequency synthesizer.

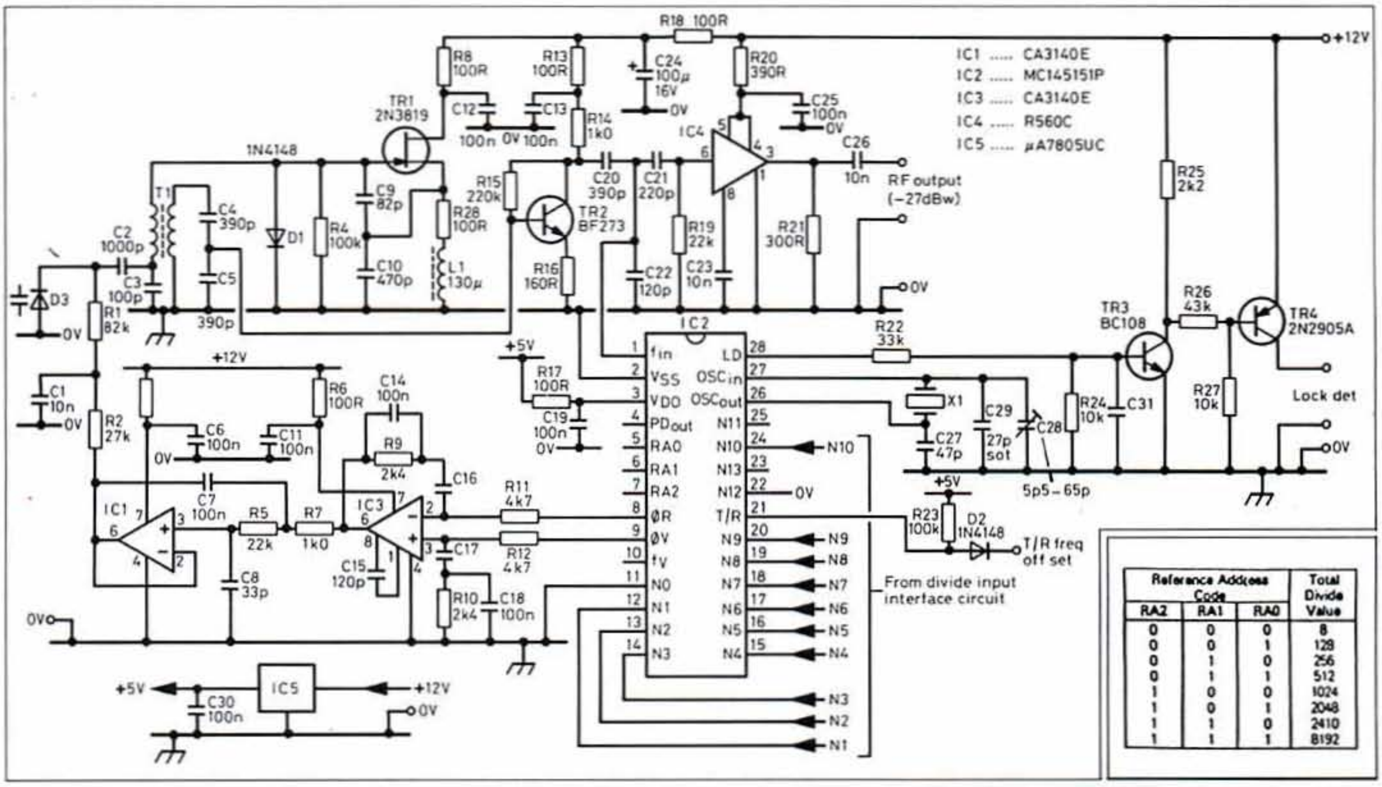


Fig 2: The synthesiser is built round an MC145151P chip controlling an FET clapp VCO.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	128
0	1	0	256
0	1	1	512
1	0	0	1024
1	0	1	2048
1	1	0	2410
1	1	1	8192

Table 1: Divide ratio inputs.

the phase detector output stabilises at a fixed voltage level. This in turn causes the VCO to stabilise at a fixed frequency, after which any slight drift will be compensated by corresponding small correctional tuning voltage level changes from the detector output. The channel spacing is related to the reference frequency, which for this circuit will be 1041.6667Hz per increment of the frequency divider. If, for example, a desired VCO frequency of 12MHz is required then the divide-by-N counter will need to be programmed to divide the desired 12MHz VCO frequency by the reference frequency.

N = VCO frequency required/Reference frequency

Where
N = Divide ratio

Therefore
N = 12,000,000/1041.6667 = 11520

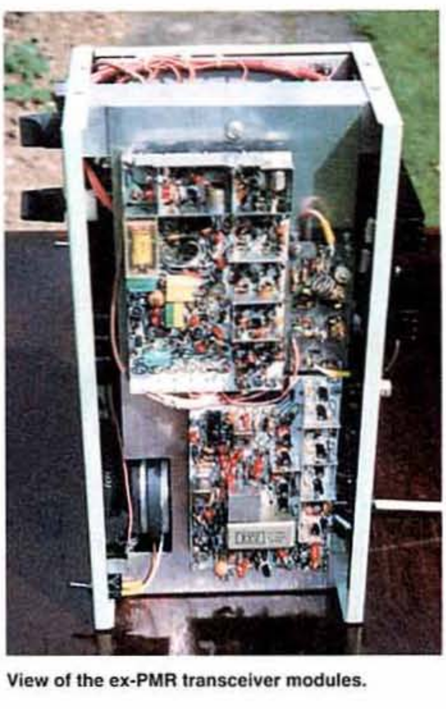
Selection of the desired ratio for the programmable divider can be achieved by manual switches. For more complex division programmes, a ROM will be necessary as a look up table, placed between the selection switches and the programmable frequency divider. The low pass filter located between the phase detector and VCO, is necessary to remove any unwanted noise that may be superimposed on the tuning voltage, and to achieve loop stability. For the circuit given, this noise will have a 1041.6667Hz component and without this filter the VCO will be frequency modulated by this noise.

MOTOROLA MC145151P INTEGRATED CIRCUIT

THE MOTOROLA MC145151P, is a parallel input, phase-locked loop (PLL) frequency synthesizer device, which employs CMOS LSI technology. This 28 pin DIL IC combines many on-chip circuit features, which only a few years ago would have occupied several additional integrated circuits. Motorola first developed and marketed the MC145151P about 12 years ago, with PMR and amateur communication equipment very much in mind.

SYNTHESIZER AND VCO CIRCUIT

THE CIRCUIT OF **FIG 2** SHOWS the dual phase ϕR and ϕV outputs, from the PLL, IC2 pins 8 and 9, which are applied to the inputs of the differential integrator IC3. This circuit has a low pass filter characteristic. The resultant DC present at the output of IC3 forms the loop-error level, or tuning voltage used to control the VCO frequency. Additional series filtering is achieved by the active low pass filter IC1 and the filter formed by resistors R1, R2 and capacitor C1, necessary to remove the remaining 1041Hz noise superimposed on the loop-error level.



View of the ex-PMR transceiver modules.

The VCO (FET TR1), is a series tuned Colpitts (Clapp) oscillator, that has a frequency range of 12MHz to 13.058MHz. However by increasing the value of C3 to 182pF, it is possible to alter the VCO frequency range to 11.108MHz - 12.1667MHz. The reason for this will become clear later on. The main frequency determining components are C3, C9, C10 and the primary winding inductance of T1, which make up a series tuned circuit. The varicap diode D3 can, for all intents and purposes, be considered to be in parallel with C3, and C2 serves as a DC blocking capacitor. The secondary winding inductance of transformer T1, and capacitors C4 and C5 make up a broadband parallel tuned circuit, centred on 12.5MHz. The VCO output appears at the junction of C4 and C5. There are two buffer amplifiers formed by transistor TR2 and IC4, that follow the VCO stage. Part of the signal output of the first buffer amplifier is fed to the F_{in} input, pin 1 of IC2. The final amplifier signal output is capable of delivering 2mW into an external 50Ω load.

Crystal X1 and associated components form the necessary external components, for the on-chip reference oscillator of IC2 (pins 26 and 27). For a final frequency resolution of 12.5kHz, a reference frequency input to the on-chip phase detector of IC2 will equal 12.5kHz/12 or 1041.6667Hz. From **Table 1**, it can be seen that by leaving the RA0, RA1 and RA2 inputs of IC2 (pins 5, 6 and 7) open circuit, the frequency of the reference crystal X1 will be:

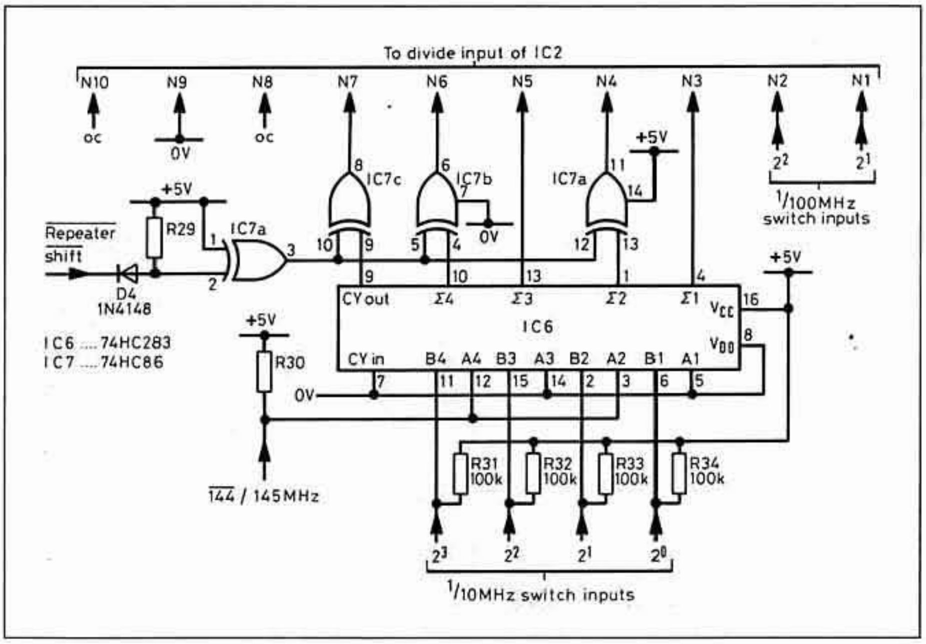


Fig 3: Divider interface. Here the receive local oscillator is *above* the signal frequency.

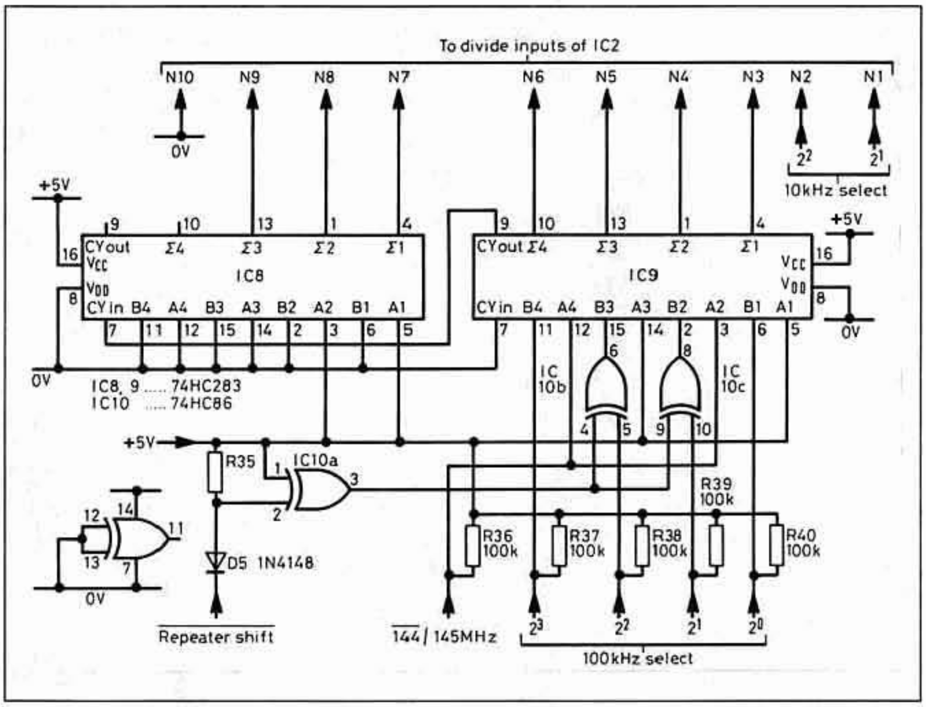


Fig 4: If the receive local oscillator is *below* the signal frequency, an additional adder is required.

X_{freq} = 1041.6667Hz x 8192
= 8.53333MHz

The Transmit/Receive offset input (IC2 pin 21) is connected to an external pull up resistor to ensure that there is sufficient current to forward bias diode D3 fully when the cathode is grounded. When the T/R input (pin 21) is at a Logic 1 state (5V), input to D2 open circuit, the programmable divider has 856 added to the count, which causes the first receive local oscillator frequency to increase (or to be offset) by 10.7MHz. This can be shown by:

Frequency Offset = 856 x 1041.6667Hz x 12 = 10.7MHz

The Lock Detect (LD) output, pin 28 of IC2, is DC amplified by two stages, formed by TR3 and TR4. Whilst the synthesizer circuit is phase locked, 12V will be present at the output of the final amplifier stage. There is sufficient output drive to energise an external relay, which could be used to over-ride the transmitter press-to-talk line to inhibit transmissions when out of lock.

INPUT DIVIDER INTERFACE

THIS CIRCUIT IS DESIGNED to enable direct frequency selections to be made using simple BCD thumbwheel-switched combinations, and as shown in **Fig 3**, it also incorporates a -600kHz repeater shift facility.

Upper and lower VCO transmit frequency limits are 12MHz and 12.16667MHz respectively, therefore the corresponding synthesizer divide ratio limits range from hex 2D00 (divide by 11520) to hex 2DAO (divide by 11680). Thus the two most significant hex digits '2D' do not change, and IC2 divide inputs N13 to N8 inclusive, can be hard wired 101101. At the divider inputs an open circuit is logic 1, and a grounded input (0V) is logic 0.

The total number of channel select switches is limited to just three, as it is unnecessary to switch the 100MHz or 1kHz decades.

For example:

To select 144.275MHz the three thumbwheel switches can be set to xx4.27x, or 145.350MHz will correspond to xx5.35x. 'x' represents the redundant switch decade positions. Only the 21 and 22 contacts of the 10kHz decade switch are utilised, and they are connected to the synthesizer divider N1 and N2 inputs. This decade switch need only be set to '0', '2', '5' and '7'. Because the ultimate channel spacing is to be 25kHz, the N0 (IC2 pin 11) divide input, which corresponds to 12.5kHz increments, is grounded.

The 100kHz frequency select switch contacts are each connected to their respective B inputs of the full adder IC6. For frequency selections below 145MHz, normally each respective adder output is fed to the synthesizer divide programme unmodified. However, for selections above 145MHz, the adder A2 and A4 inputs will be at logic 1 (5V) level, which causes hex A (binary 1010) to be added to the 100kHz switched select frequency data. The overall effect is to add hex 50 (further divide by 80) to the synthesizer programme divide inputs, N7 to N0.

When the repeater shift input at D4 is grounded, the XOR gates of IC7 will invert the divide selection data at IC2 divide inputs N7, N6 and N4. The overall effect is to subtract hex 30, (divide by 48) from the input selection data at inputs N7 to N0, which in turn reduces the transmit frequency by 600kHz from that selected by the thumbwheel switches.

It is important that the off-board circuitry be arranged so that a selected repeater shift can only occur when a frequency of 145MHz and above is selected, and only on transmit. The receive mode (Fig 2) is activated when the T/R input at diode D2 is active low, this causes the receiver first local oscillator frequency to step up 10.7MHz.

DIVIDE INTERFACE - LOWER IF OPTION

THE CIRCUIT OF **FIG 4** IS suggested as an alternative to that of Fig 3, where the receive first local oscillator tracks 10.7MHz *below* the received signal frequency. The upper and lower tracking frequency limits of the receiver local oscillator will now be 133.3MHz and 135.3MHz. To achieve this, the channel select data present at the programme divide inputs of the synthesizer IC2, will be hex 2A48 (divide by 10824) to hex 29A8 (divide by 10664), therefore the programme divide inputs N13 to N10 should be hard wired to 1, 0, 1 and 0 respectively. An additional full adder is required, and the XOR gate circuits which form part of the repeater shift facility, are placed between the adder IC9 and the channel switches. Lastly the T/R input logic at diode D2, (**Fig 2**) will be reversed, an active low is required for transmit mode.

. . . to be concluded

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THIS CIRCUIT HAS BEEN designed to ensure that it is impossible to transmit spurious interference whilst the synthesizer is out of phase lock. All synthesizers become unstable for very short periods when changing from one frequency to another, the worst possible case for my synthesizer design is approximately 0.25 seconds.

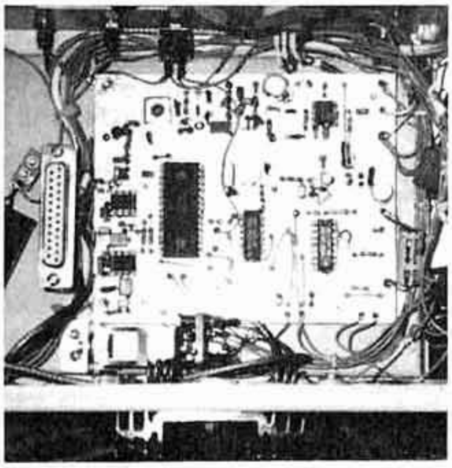
The circuit is shown in **Fig 5**, with relay RLA energised by the +12 volts present at the synthesizer module lock detect output. Capacitor C31 removes any transient noise from this supply, which can especially be present during channel changes. Diode D6 offers back EMF protection for transistor TR4 (located on the synthesizer module). Whilst relay RLA is energised the PTT input circuit is completed via relay contacts A1 and diode D7 to the base of transistor TR5. With the microphone PTT switch open circuit, transistor TR5 will fully conduct, therefore the Tx/Rx output will be 0V (short circuit). The repeater output derived at the junction of contacts A1 and diode D8 will be high (open circuit). Transistor TR6 is fully forward biased and completes the charging current circuit, via diode D8. Transistor TR7 is also fully conducting, permitting Relay RLB to be fully energised.

When the microphone PTT switch is closed, TR5 ceases to conduct, the repeater output becomes low (short circuit to 0V/Ground), the Tx/Rx offset output becomes high (+12v) and transistor TR6 switches off. TR7 will continue to conduct until capacitor C33 has sufficiently discharged via resistors R44 and RV1 after which RLB de-energises. The discharge time for capacitor C33 is adjustable by pre-set resistor RV1. The relay contacts B1 switch +12V between the transmitter and receiver circuits. The adjustment of RV1 should be such that the relay B1 change over contacts inhibit the transmitter +12V supply sufficiently until the synthesizer is returned to the phase lock condition.

Should the synthesizer develop a permanent fault such that a continuous out of lock condition exists, +12V from the phase detect output will be removed, causing RLA to become de-energised. Opening relay contacts A1 will break the PTT input circuit, which prevents any further transmission.

CONSTRUCTION AND TESTING

CONSTRUCTION AND TESTING should not present too many problems for those used to building their own equipment. The component layout was not found to be all that critical, which can be borne out by the fact that I built several prototypes, each with a slightly varied component layout, and all worked first time.



A view of the synthesizer/VCO board. The highly versatile MC145151P chip can be clearly seen.

Although the final product was assembled on a purpose built printed circuit board, measuring 120 x 120mm, an alternative method might be to construct the circuit as two separate modules. The first module could contain the VCO and Buffer circuits, based on the printed circuit board, whereas the second module could contain the synthesizer, filter circuits and the divider interface. The second module could be assembled on Veroboard.

After assembly, before applying power, carefully check the circuits to ensure that there are no wiring errors. After power up check that the reference oscillator is working correctly, adjust the trimmer capacitor VC28 to obtain a frequency counter indication of 8.5333MHz. To achieve this result it may be necessary to change the given value of C29 by the select-on-test method. An HF receiver with an accurately calibrated frequency read out may suffice in place of the frequency counter for this and further frequency checks. Check that the VCO is functioning, which will be apparent by a terminal output waveform whose frequency will range from about 10MHz to about 13MHz.

Connect a DC voltmeter, set to the 10 volt range, between the junction of resistors R1 and R2 and ground. Note the loop-error signal voltage levels at channel sections of 144MHz (transmit mode) and 146MHz (receive mode), the voltmeter should indicate about 2VDC and 8VDC respectively. To achieve this result it may be necessary to adjust the core of T1. In the case of the lower IF option, or if the Varicap D3 has been substituted by another type, it may be required to change the value of capacitor C3 to obtain the correct test results. Reconnect the DC voltmeter to the output terminals of the lock detect driver stages, note that the voltmeter indicates 12VDC. Place a short circuit between the junction of resistors R1 and R2 and ground, and observe that the voltmeter reading falls to 0V.

AIR TESTING THE FINISHED PRODUCT

THE COMPLETED PRODUCT met all the technical requirements that I set out to achieve, but with one very minor exception. There was

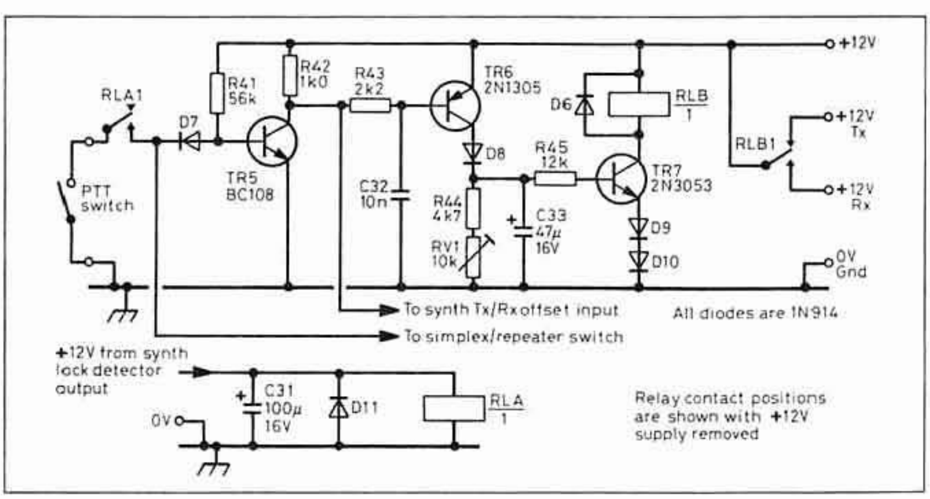


Fig 5: The push-to-talk interface. Transmissions are inhibited if the synthesizer is out of lock.

COMPONENTS LIST

SYNTHESIZER AND VCO

Resistors

All 0.25W 5%

R1	82k
R2	27k
R3	100R
R4	100k
R5	22k
R6	100R
R7	1k
R8	100R
R9	2.4k
R10	2.4k
R11	4.7k
R12	4.7k
R13	100R
R14	1k
R15	220k
R16	160R
R17	100R
R18	100R
R19	22k
R20	390R
R21	300R
R22	33k
R23	100k
R24	10k
R25	2.2k
R26	43k
R27	10k
R28	100R

Capacitors

All values are microfarads unless otherwise stated. All are miniature types.

C1	0.01 polycarbonate
C2	1000pF ceramic
C3	100pF ceramic
C4	390pF ceramic
C5	390pF ceramic
C6	0.1 polycarbonate
C7	0.1 polycarbonate
C8	0.033 polycarbonate
C9	82pF ceramic
C10	470pF ceramic
C11	0.1 polycarbonate
C12	0.1 polycarbonate
C13	0.1 polycarbonate
C14	0.1 polycarbonate
C15	120pF ceramic
C16	1 polycarbonate
C17	1 polycarbonate
C18	0.1 polycarbonate
C19	0.1 polycarbonate
C20	390pF ceramic
C21	220pF ceramic
C22	120pF ceramic
C23	0.01 polycarbonate
C24	100 16V electrolytic
C25	0.1 polycarbonate
C26	0.01 polycarbonate
C27	47pF ceramic
C28	5.5 to 65pF trimmer
C29	27pf SOT ceramic
C30	0.1 polycarbonate

Note: Lead spacing for polycarbonate capacitors, 0.1 and 0.01 is 2.5mm. For the 1.0 capacitor the lead spacing is 5mm.

Inductors

T1	Toko KANK3334
L1	130μH fixed 5mm lead spacing

Semiconductors

TR1	2N3819
TR2	BF274/BF273
TR3	BC108
TR4	2N2905A

Integrated Circuits

IC1	CA3140E
IC2	MC145151P Stockists: Cirkit etc.
IC3	CA3140E
IC4	R560C
IC5	UA7805UC

Diodes

D1,D2	IN4148
D3	MVAM115 (or near equiv. ½ BB212)

IC Sockets

28-way DIL	Qty 1
8-way DIL	Qty 3

Crystal

Crystal X1	8.5333MHz Type HC25U Quartslab

HIGHER IF OPTION

Resistors

All 0.25W 5%

R29	100k
R30	100k
R31	100k
R32	100k
R33	100k
R34	100k

Diodes

D4	1N4148

Integrated Circuits

IC6	74HC283
IC7	74HC86

Stockists: Cirkit, Maplin etc.

IC Sockets

16way DIL	Qty 1
14way DIL	Qty 1

LOWER IF OPTION

Resistors

All 0.25W 5%

R35	100k
R36	100k
R37	100k
R38	100k
R39	100k
R40	100k

Diodes

D5	1N4148

Integrated Circuits

IC8	74HC283
IC9	74HC283
IC10	74HC86

Stockists Cirkit, Maplin etc.

IC Sockets

16way DIL	Qty 2
14way DIL	Qty 1

PRESS-TO-TALK INTERFACE

Diodes

D6,7,8,9,10 1N914

Transistors

TR5	BC108
TR6	2N1305
TR7	2N3053

Resistors

All 0.25W 5%

R41	56k
R42	1k
R43	2.2k
R44	4.7k
R45	12k

Variable Resistor

RV1 10k linear

Capacitors

C31	100μF 16VW electrolytic
C32	0.01μF mono
C33	47μF 16VW electrolytic

Relays

RLA	micro min. (eg Maplin stock No BK47B)
RLB	12 Volt min. SPCO (eg Maplin stock No JM18U)

some slight synthesizer noise (1041Hz) on the transmitted carrier, although this was not sufficient to cause any unsolicited comments on the subject from other participating amateurs during the course of these trials. I also found that voltage transients present on the +12 volt supply rail, especially when switching from receive to transmit, can cause momentary loss of synthesizer lock, but this problem was easily overcome by placing a 1000μF electrolytic capacitor across the supply rail.

CONCLUSION

THE TOTAL SYNTHESIZER module component cost was about £40, but by using salvaged components and shopping around where possible I am sure that there is scope for reducing this cost by at least five pounds. Without doubt the most difficult part of the development was the low pass filter circuitry.

This task would have been much easier had I opted for an overall 25kHz channel spacing (2083.3334 Hz reference frequency), but this would have ultimately resulted in a 21.4MHz transmit-receive offset, utilising the Tx/Rx offset facility of the Motorola MC145151P IC.

REFERENCES:

(1) Motorola MC145151 product data sheet (dated 1980).